11. (Amended) A moving image signal coding apparatus [of moving image signal] of claim 10, wherein said predicted image combining means issues a predicted image produced from the latest decoded frame in time out of the at least two or more predicted images compensated of motion by said at least two [or more] motion vectors for use in coding of the present processing pixel block.

B1 cancel

REMARKS

After the foregoing Amendment, claims 1-11 are pending in the present application. Claims 1-11 have been amended to more particularly point out indistinctly claim the subject matter which Applicant regards as the invention.

In regards to the objections made to the drawings, Applicant has attached herewith, a copy of the Preliminary Amendment filed on June 15, 1998. Formal drawings will be submitted upon receiving a Notice of Allowability. Applicant submits that no new matter has been added to the application by the amendment.

THE PRESENT INVENTION

The present invention provides a method of decoding a moving image signal. The image signal is a stream of pixel blocks segregated into image frames and at least two decoded image frames are temporarily stored in a memory. The method includes decoding at least two motion vectors relating to a present pixel block of the stream of pixel blocks of a present frame. The motion of the at least two previously decoded image frames stored in memory is compensated with respect to a corresponding one of the at least two motion vectors. A predicted image is generated from each of the at least two previously decoded image frames for reconstructing the present pixel block of the present frame. In this way, the predicted image used in reconstruction of the present pixel block is selected depending on the presence or absence of decoding error contained in the two or more predicted images.

REJECTIONS UNDER 35 U.S.C. § 102

The Examiner has rejected claims 1-6 and 9 under 35 U.S.C. § 102 as being unpatentable over U.S. Patent No. 5,737,022 (Yamaguchi et al.) The Examiner contends that Yamaguchi disclose a variable length code decoding means, a motion compensation means, a bit error detecting means, and a predicted image selecting means in accordance with the Applicant's claims. Applicant respectfully traverses the rejection.

Amended claim 1 recites, *inter alia*, a method of decoding a moving image signal wherein the signal is decoded by the steps of

"decoding at least two motion vectors relating to a pixel block of the stream of pixel blocks of a present frame;

compensating the motion of at least two previously decoded image frames stored in a memory with respect to a corresponding one of the at least two motion vectors;

generating a predicted image from each of the at least two previously decoded image frames for reconstructing the pixel block of the present frame..."(emphasis added)

Yamaguchi et al. disclose a motion picture error concealment and compensation method. The concealment method is directed to concealing packets of an ATM cell lost by packet discarding or transmission line error.

The motion compensation means (elements 113, 141, and 144) shown in Fig. 7 operates in the following manner. The motion compensation means conceals a pixel block X (as shown in Fig. 8) by storing adjacent pixel blocks (i.e., blocks A-H in Fig. 8) of an image in a frame memory 130. A concealment circuit creates a prediction value for use of motion compensation information of decodable blocks among the blocks A-H. Thus, a prediction value is derived for a pixel near the block X from the reference image (blocks A-H) read out from the frame memory 130. Then, a motion compensation error evaluation circuit 142 calculates an error evaluation value between the read out reproduced image and a prediction value of a pixel block adjacent to the block X. The error evaluation value is provided to a selection circuit 143. The selection circuit 143 selects the motion compensation prediction value having a minimum error for use in concealing block X.

A second motion compensation circuit 144 creates a motion compensation prediction value of the block X based on a reference image signal read out from the frame memory 130. If the block X is detected to be a decodable block, a selector 150 outputs a signal corresponding to the block X stored in the frame memory 130 via a feedback line 60. If a block is a non-decodable block, a concealment image (in a position corresponding to the block X) from a previously stored frame is supplied from the second motion compensation prediction circuit 144 via the line 60.

In this way, the error in reception of block X is concealed by predicting block X by way of adjacent blocks and motion vectors of the same frame, or, by simply replacing block X with a corresponding block of a previously stored frame. Yamaguchi et al. do not disclose or suggest reconstructing a pixel block of a present frame by applying motion vectors of the present frame to previously decoded frames stored in memory as recited in Applicant's amended claim 1.

Accordingly, Applicant respectfully requests that the rejection of claim 1 under 35 U.S.C. § 102 be withdrawn.

Claim 2 is directly dependent upon claim 1, and therefore, is allowable over Yamaguchi et al. for at least the same reasons discussed above.

Independent claims 3-5 recites substantially the same limitation as discussed above with reference to claim 1. Namely, that the motion vectors of a present processing pixel block of a frame are applied to previously decoded frames stored in memory for reconstructing a pixel block of the present frame. Likewise, Applicant submits that claims 3-5 are allowable at least for the same reasons discussed above. Thus, Applicant respectfully requests that the rejection of claims 3-5 under 35 U.S.C. § 102 be withdrawn.

Claim 6 is directly dependent upon claim 5 and therefore, is allowable over Yamaguchi et al. at least for the same reasons.

Amended claim 9 recites, *inter alia*, a moving image signal coding apparatus including "motion compensation means for issuing plural predicted

images based on stored images from the output of said motion vector detecting means..."

As discussed above, Yamaguchi et al. do not disclose reconstructing a pixel block of a present frame by the application of motion vectors of the present frame to previously decoded frames , but rather, applying motion vectors to adjacent pixel blocks. Accordingly, Applicant respectfully requests that the rejection of claim 9 under 35 U.S.C. § 102 be withdrawn.

In view of the above, Applicant respectfully requests that the rejection of claims 1-6 and 9 under 35 U.S.C. § 102 be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 103

The Examiner has rejected claims 7 and 8 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,737,022 (Yamaguchi et al.) The Examiner contends that although Yamaguchi does not specifically disclose the memory being configured in a map format, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamaguchi et al. to arrive at the Applicant's invention. Applicant respectfully traverses the rejection.

Applicant submits that since independent claim 5 has been shown to be allowable with respect to the cited reference, claims 7 and 8 are allowable, at least by their direct or indirect dependency upon claim 5. Accordingly, Applicant respectfully requests that the rejection of claims 7 and 8 under 35 U.S.C. § 103 be withdrawn.

The Examiner has rejected claims 10 and 11 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,737,022 (Yamaguchi et al.) The Examiner contends that although Yamaguchi does not specifically disclose a predicted image combining means, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamaguchi et al. to arrive at the Applicant's invention. Applicant respectfully traverses the rejection.

Applicant submits that since independent claim 5 has been shown to be allowable with respect to the cited reference, claims 10 and 11 are allowable, at

least by their direct or indirect dependency upon claim 9. Accordingly, Applicant respectfully requests that the rejection of claims 10 and 11 under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

In view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including claims 1-11, is in condition for allowance, and such action is respectfully requested at an early date.

Respectfully Submitted,

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Lawrence E. Ashery